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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,964	01/10/2002	Frederic Reblewski	109893-130276	6410

25943 7590 11/07/2003

SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITES 1600-1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/043,964	REBLEWSKI ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02/05/2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to applicants' Amendment and Remarks accompanying RCE filed on 08/25/2003 regarding application 10/043,964 filed on 01/010/2002. New additional Claim 25 is added. Claims 1 – 25 remain pending.

Claim Objections

2. Claims are objected to because of the following informalities:

Claim 7, line 3 – 4, change "the memory element" to **—said at least a memory element—**.
Claim 7, line 5, change "the crossbar device" to **—said each crossbar device—**.
Claim 7, line 6, change "buffers" to **—buffer—**.
Claim 7, line 6 – 7, change "the memory elements" to **—said at least a memory element—**.
Claim 7, line 7, change "buffers" to **—buffer—**.
Claim 25, line 1, change "Vdd" to **—said raised threshold voltage over Vdd—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 15 – 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 15, line 5, the phrase "*a same know logic value*" renders the claim unclear whether *the know logic vale* is *zero*, *one* or a value between zero and one. Claim 15, line 5 – 7, the phase "*to facilitate reduction of current drain by reducing contention on outputs of said plurality of output buffers*" renders the claim unclear. Which component's current drain is reduced? What applicants intend to mean *reducing contention on outputs of said plurality of output buffers*? Clarification of the claim language is required.

Other dependent Claims16 – 24 that are not specifically cited above are also rejected because of the deficiencies of their respective parent claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 – 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to *Sample et al.* in view of U.S. Patent No. 5,644, 496 to *Agrawal et al.*

6. As to Claim 1 – 6, *Sample et al.* shows in Fig. 13 D partial structure of a hybrid between crosspoint-type crossbar 650 and multiplexer-type crossbar 630 (Fig. 13 D; col. 12, line 61 – col. 13, line 20). Notice that a complete crossbar device contains a plurality of crossbar structures as shown in Fig. 13 D. The complete configurable crossbar device can have *n input lines* and *m output lines* – [Claim 1].

Sample et al. do not teach a method of placing a *pass transistor* at the *input port* of each input line to control inputting the data into the multiplexer-type *crossbar*. But, *Agrawal et al.* teach this method.

Agrawal et al. show in Fig. 6A inserting a *PIP 521* (i.e., programmable interconnect switch) between input buffer 516 and an input line of *UPM 501* (i.e., user programmable multiplexer). The *PIP 521* is consisted of a *pass transistor 35* which is

controlled/configured by a *memory cell 36* as shown in Fig. 2A. The *UPM 501* in Fig. 6A is a *multiplexer-type crossbar*. Notice that the *PIP 521* is an *input data switch*, which is installed at the *input port* of *crossbar device* (*UMP 501*) in order to *control timing* for *selectively feeding appropriate data* into the *crossbar device* thereby improving the performance of the *crossbar device*.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of *Agrawal et al.* by inserting an *input data switch* (*PIP 521*) at each *input port* of *crossbar device* (*UMP 501*) in order to *control timing* for *selectively feeding appropriate data* into the *crossbar device* thereby improving the performance of the *crossbar device* as recited in Claims 1 – 4 and 6.

Sample et al. teach using a *2-to-4 decoder 640* for coupling the *input lines* of a *partial crossbar device 630* in order to control its output. The complete configurable crossbar consists of a plurality of *crossbar devices 630*; therefore it has a plurality of 2-to-4 decoders 640 – [Claim 5].

For reference purposes, the explanations given above in response to Claims 1 – 6 are called **[Response A]** hereinafter.

7. Claims 7, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to *Sample et al.* in view of *applicants' admitted prior art* and U.S. Patent No. 6,175,952 to *Patel et al.*

8. As to Claim 7, *Sample et al.* show in Fig. 13D a crossbar device. *Sample et al.* do not teach installing an output buffer at each output line. But it is well known in the art and also is a *digital data-transmission standard* that, to adjust signal outputting from *one digital data device* to an *acceptable level* before feeding into *another digital data device*, an *output buffer* should be installed at *each output port* of each *digital data device*. This fact is shown in applicant's admitted prior arts in Figs. 1a, 2 and 3. With this *output buffer* in place at location pointed by reference numeral 620 in Fig. 13D, first subject matter in the claim is achieved. Notice that the *memory element 652* is electrically associated with the *output buffer*, which can be connected at a location indicated by 620.

Sample et al. also do not teach *voltage supply structure* as recited in the claim. However, *Patel et al.* teach this subject matter in Fig. 23 (col. 25, line 56 – col. 26, line 26; col. 26, line 43 – 55). Notice that the *cross-coupled latch 2310* in Fig. 23 is an *output buffer* and its voltage is at a *VCC1* (e.g., *Vdd*) level. *Patel et al.* teach that the *isolation device 2315* in Fig. 23, which is an *output switch* 2315 containing a *pass-transistor* 2320 (col. 26, line 43 – 55), and its *supply voltage VCC2* can be coupled from an *internal circuitry* of the integrated circuit (col. 24, line 63 – 64). *Patel et al.* also teach that, in order to achieve (i.e., maintain) *output signal* at a desired VCC (i.e., Vdd) level, the *bias supply voltage* (VCC2) of a *pass-transistor* of *output switch* should be at about VCC + |Vth| level, where |Vth| is a threshold voltage (col. 13, line 61 – 63; col. 13, line 36 – 44). It is indicated in Fig. 1b of *applicants' admitted prior art* that the *supply voltage* of *pass transistor* is coupled from a *memory element 104*.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of *Patel et al.* and *applicants' admitted prior art* (Fig. 1b) to set the *supply voltage* of a *pass-transistor* of *output switch* to a level of VCC + |Vth| in order to achieve maintain *output signal* at a desired VCC (i.e., Vdd) level.

Patel et al. teach the *voltage supply structure* in Fig. 23, which has similar components (i.e., *pass-transistor* 651 and *output buffer*) as that disclosed by *Sample et al.* (Fig. 13D) and *applicants' admitted prior art* (Fig. 2). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the teachings of *applicants' admitted prior art* on *output buffer* and teachings of *Patel et* al. on *voltage supply structure* mentioned above, all the subject matters recited in the claim can be achieved.

For reference purposes, the explanations given above in response to Claim 7 are called **[Response B]** hereinafter.

9. As to Claims 13 and 14, *Sample et al.* teach that the *crossbar* is an integrated circuit device (abstract). *Patel et al.* teach that the *voltage supply structure* is designed in an integrated circuit (abstract). Therefore, reconfigurable crossbar device can be a stand-

alone integrated circuit design or a building block (i.e., block of an integrated circuit) being integrated with other devices to provide data cross-connect functions.

10. Claims 8 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to *Sample et al.* in view of *applicants' admitted prior art*, U.S. Patent No. 6,175,952 to *Patel et al.* and U.S. Patent No. 5,644, 496 to *Agrawal et al.*

11. As to Claims 8 – 12, *Sample*, *applicants' admitted prior art* and *Patel et al.* (called Sample_Patel et al. hereinafter) teach all the subject matters except a method of inserting a *pass-transistor* and *control memory element* at each input line. But *Agrawal et al.* teach this method as explained in **[Response A]** given above.

Due to the same reasons included in **[Response A]** and **[Response B]** given above, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of *Agrawal et al.* and to apply teachings of Sample_Patel et al. to achieve all the subject matters recited in Claims 8 – 12.

Allowable Subject Matter

12. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 25 is allowed is because that the prior arts do not teach or suggest the following subject matters:

- The reconfigurable logic circuit of Claim 7 wherein provision of the raised threshold voltage over Vdd at the input voltage of the output buffer is to facilitated reduction of parasitic current flowing through a first inversion stage of the buffer as recited in Claim 25.

Response to Amendment and Remarks

12. Applicants' argument files 08/25/2003 accompanying the RCE have been fully considered but they are not all persuasive. Key non-persuasive arguments and their

responses are summarized and given below. Notice that examiner only focuses his examination on the languages and limitations (i.e., scope) recited by the claims.

[Argument 1] Examiner's prior art *does not* disclose *placing a pass transistor at the input port of each input line* to control inputting data into the multiplexer.

[Response 1] Applicants do not include the limitation of *placing a pass transistor at the input port of each input line* in Claims 1 – 6. Applicants only claim that *each pass transistor is coupled to an input line*, therefore, the pass transistor can be installed at any location on the input line.

[Argument 2] Examiner's prior art teach a *step-down voltage supply structure* instead of a *step-up voltage supply structure* as claimed by applicants.

[Response 2] Examiner's prior art does teach a *step-up voltage supply structure*. Detailed explanations are included in **[Response B]** given above.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (703) 308-4916. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Art Unit 2825
November 3, 2003

VUTHE SIEK
PRIMARY EXAMINER